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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,731	09/18/2003	Shunpei Yamazaki	0553-0187.01	5614

7590 11/30/2005

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EXAMINER	
COLON, GERMAN	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,731	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	German Colón	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *60,62-65,67-71,73-76 and 78-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *60,62-65,67-71,73-76 and 78-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/587,369.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The Amendment, filed on September 15, 2005, has been entered and acknowledged by the Examiner.

2. Cancellation of claim 77 has been entered.

3. Addition of claims 79-81 has been entered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 65, 67, 69 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US 6,239,470) in view of Yudasaka (US 6,359,606), further in view of Kuribayashi et al. (US 6,215,244).

Regarding claim 65, Yamazaki discloses a method of manufacturing a display device comprising the steps of:

forming a plurality of TFTs over a substrate **101**;

forming an insulating film **114** comprising a resin over the plurality of TFTs;

forming a first passivation film **116** over the insulating film (see Col. 4, lines 26-27); and

forming a first electrode **117** over and in contact with the passivation film. Yamazaki teaches this structure to be used for driving an EL display (see at least Col. 1, lines 10-14) but is silent regarding the components of the EL display.

However, in the same field of endeavor, Yudasaka discloses an organic EL element comprising a first electrode, a light emitting layer formed on the first electrode by an ink jet method (see Col. 9, lines 5-7) and a second electrode formed on the light emitting layer, wherein the EL element is driven by an active matrix device comprising a plurality of TFTs. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an EL layer and a second electrode to the device of Yamazaki since Yamazaki teaches the desirability of using the device for driving an EL display. Further, Yudasaka teaches to be conventional and well known in the art to drive an EL display with a device comprising a plurality of TFTs. Moreover, EL displays require a light-emitting layer sandwiched between two electrodes.

Yamazaki-Yudasaka discloses the claimed invention except for the limitation of "forming a second passivation film over the EL element". However, Yudasaka discloses an EL display having a passivation film made of silicon nitride over an electroluminescent element with the purpose of inhibiting the deterioration of the device by protecting the EL element from oxygen and moisture (see Col. 10, lines 65-67, in view of Col. 1, lines 50-53 and Col. 6, lines 55-57). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a passivation film over the electroluminescent element in order to inhibit the deterioration of the device by protecting the EL element from oxygen and moisture.

Yamazaki-Yudasaka discloses the claimed invention except for the limitation of the EL element being formed in succession without exposure to an atmosphere. However, Kuribayashi discloses a method of manufacturing a display device and teaches to form the plurality of layer comprising the EL element in succession without exposure to an atmosphere in order to achieve continuous, stable, high-luminance light emission over a long period (see at least Col. 17, lines 1-11). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the EL element in succession without exposure to an atmosphere, with the purpose of achieving continuous, stable, high-luminance light emission over a long period.

Regarding claim 67, Yamazaki-Yudasaka discloses each of the first and second passivation films comprising SiN (see `470, Col. 4, lines 26-27; and `606, Col. 10, lines 65-67).

Regarding claim 69, Yamazaki discloses an insulating film comprising SiO_2 between the substrate and the plurality of TFT. However, the reference discloses the suitability of SiN as an insulating layer (see Col. 3, lines 63-65). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use SiN instead of SiO_2, since Yamazaki teaches the suitability of the former to replace SiO_2 as an insulating layer.

Regarding claim 75, Yamazaki-Yudasaka-Kuribayashi discloses a device and a method of manufacturing said device, comprising (see Fig. 2C of `470):

forming a TFT over a substrate **101**;

forming a first insulating layer **112** comprising SiN or SiO_xN_y over the TFT;

forming a leveling film **114** comprising a resin over the first insulating film;

forming a second insulating film **116** comprising SiN;

forming a light emitting element (see US `606) over the second insulating film, said light emitting element comprising a first electrode in contact with the second insulating film, a second electrode and an organic EL material interposed therebetween; and

forming a third insulating layer comprising SiN (see **60** in `606),

wherein the light emitting layer, the second electrode and the third insulating film are formed in succession without exposure to an atmosphere (see Col. 17, lines 1-11, in `244). Same reasons for combining stated in claim 65 apply.

6. Claims 68 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki-Yudasaka-Kuribayashi as applied to claim 65 above, and further in view of Kikukawa et al. (US 6,329,036).

Regarding claim 68, Yamazaki-Yudasaka-Kuribayashi discloses the passivation layers comprising silicon nitride, but is silent regarding the limitation of said layers comprising Si, Al, N, O and a rare earth element.

However, Kikukawa discloses a semiconductor device comprising an insulating film, and teaches a silicon nitride film and a rare earth-containing SiAlON film as art recognized equivalent materials. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a rare earth-containing SiAlON film, as disclosed by Kikukawa, instead of a silicon nitride film, as disclosed by Yamazaki-Yudasaka-Kuribayashi, since Kikukawa teaches both films to useful insulating materials and art recognized equivalents (see Col. 8, lines 9-13). Further, it has been held to be within the general skill of an artisan to

select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

Regarding claim 70, claim 70 is rejected over the reasons stated in the rejection of claim 68.

7. Claims 60, 62-64, 71, 73 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (US 6,303,963) in view of Yamazaki (US 6,239,470).

Referring to claims 60 and 71, Ohtani discloses a method of manufacturing a display device (see Figs. 18 and 20) comprising the steps of:

forming a plurality of TFTs **3503** over a substrate **3501**;

forming an insulating (and/or leveling) film **3608** comprising a resin over the plurality of TFTs;

forming an EL element over the insulating film, said EL element comprising a first electrode **3616** formed in contact with the insulating film, a light emitting layer **3618** formed over the first electrode by an ink jet method (see Fig. 20 in view of Col. 24, lines 60-64) and a second electrode **3620** formed over the light emitting layer,

wherein the first electrode is electrically connected to one of said TFT through a contact hole through the insulating layer; and

wherein the light-emitting layer is in contact with the insulating layer. Ohtani is silent regarding the limitation of the display device driving means including a plurality of TFTs, an insulating film comprising a resin, *and* a passivation film over the insulating film.

However, Yamazaki discloses means for driving a display device comprising:

a plurality of TFTs over a substrate **101**;

forming an insulating film **114** comprising a resin over the plurality of TFTs;

forming a passivation film **116** *over* the insulating film (see Col. 4, lines 26-27); and teaches this embodiment to provide a configuration which reduces the problem of generation of a capacity between a masking film and the transistors, which adversely affect the operation of said transistors (see at least Col. 1, lines 31-35; and Col. 5, lines 59-60). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the driving means of Yamazaki in the device of Ohtani, with the purpose of reducing the generation of a capacity between a masking film and the transistors, resulting in improved driving of the display. Accordingly, Ohtani-Yamazaki discloses the anode and the EL layer in contact with the passivation film.

Referring to claims 62, 63 and 73, Ohtani-Yamazaki discloses the passivation film **116** comprising SiN (see Col. 4, lines 26-27 of `470).

Referring to claim 64 and 74, Ohtani discloses the light emitting layer comprising an organic material (see Col. 24, lines 60-64).

8. Claims 76 and 79-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani-Yamazaki as applied to claim 60 above, and further in view of Yudasaka (US 6,359,606).

In regards to claim 76, Ohtani-Yamazaki discloses the claimed invention (see Fig. 2C of `470) including the steps of:

forming a TFT over a substrate **101**;

forming a first insulating layer **112** comprising SiN or SiO_xN_y over the TFT;

forming a leveling film **114** comprising a resin over the first insulating film; and

forming a second insulating film **116** comprising SiN. Ohtani-Yamazaki is silent regarding the limitation of "forming a third insulating film over the second electrode".

However, Yudasaka discloses an EL display having an insulating film made of silicon nitride over an electroluminescent element with the purpose of inhibiting the deterioration of the device by protecting the EL element from oxygen and moisture (see Col. 10, lines 65-67, in view of Col. 1, lines 50-53 and Col. 6, lines 55-57). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an insulating film over the electroluminescent element in order to inhibit the deterioration of the device by protecting the EL element from oxygen and moisture.

In regards to claims 79-80, Ohtani-Yamazaki discloses the first and second insulating films comprising SiN and/or SiO_xN_y (see '470 and materials disclosed).

In regards to claim 81, the claim is rejected over the reasons stated in claim 76.

9. Claim 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani-Yamazaki-Yudasaka as applied to claim 76 above, and further in view of Tang et al. (US 5,684,365).

Ohtani-Yamazaki-Yudasaka discloses the claimed invention except for the limitation of forming a storage capacitor.

However, in the same field of endeavor, Tang discloses an organic EL device (see Fig. 3) comprising a plurality of TFTs, wherein a storage capacitor is formed with the purpose of enabling the excitation power to an addressed EL element to stain on once it is selected; thus the

circuit provides a memory that allows the EL element to operate at a duty cycle close to 100%, regardless of the time allotted for addressing (see at least col. 6, lines 16-20). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a storage capacitor to the device of Yamazaki-Yudasaka, in order to enable the excitation power to an addressed EL element to stain on once it is selected; thus the circuit provides a memory that allows the EL element to operate at a duty cycle close to 100%, regardless of the time allotted for addressing.

Response to Arguments

10. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to German Colón whose telephone number is 571-272-2451. The examiner can normally be reached on Monday thru Thursday, from 8:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc

JOSEPH WILLIAMS
PRIMARY EXAMINER